What is claimed is:

1. A semiconductor transistor comprising:

a semiconductor substrate of a first conductivity type having a top surface;

a source region of a second conductivity type; opposite the first conductivity type in the semiconductor substrate;

a drain region of the second conductivity type spaced from the source region in the semiconductor substrate;

a trench having substantially upright vertical sidewalls and a bottom surface, at a desired depth below the top surface, formed in the semiconductor substrate intermediate the source and drain regions which are disposed at depths in the substrate approximately greater than the desired depth of the trench;

a channel region formed beneath the bottom surface of the trench and immediately contiguous the source and drain regions;

a trench-to-gate insulating layer formed in the trench;

a trench floating gate electrode; formed on the trench-to-gate insulating layer inside the trench and having a top surface;

an inter-gate dielectric layer formed on the top surface of the trench floating gate electrode; and

a control gate electrode formed on the inter-gate dielectric layer.

2. The semiconductor transistor of claim 1 wherein the trench-to-gate insulating layer further comprises:

a trenched gate dielectric spacer formed on the substantially upright vertical sidewalls inside the trench: and

a trenched gate tunneling dielectric formed on the bottom surface inside the trench.

3. The semiconductor transistor of claim 1 wherein the trench-to-gate insulating layer is thicker on the substantially upright vertical sidewalls inside the trench than on the bottom surface inside the trench.

4. The semiconductor transistor of claim 1 further comprising:

sidewall dopings of the first conductivity type disposed immediately contiguous the substantially vertical sidewalls of the trench and laterally spacing each of the source and drain regions from the trench.

5. The semiconductor transistor of claim 1 wherein the source region and drain region are formed by a self-limited lateral diffusion process.

6. The semiconductor transistor of claim 1 wherein the source region and drain region are each disposed contiguous portions of the sidewalls and the bottom of the trench.

7. The semiconductor transistor of claim 1 wherein the top surface of the trenched gate electrode is substantially planar to the top surface of the semiconductor substrate.

8. A semiconductor transistor comprising:

a semiconductor substrate of a first conductivity type having a top surface:

a source region of a second conductivity type opposite the first conductivity type in the semiconductor substrate:

a drain region of the second conductivity type spaced from the source region in the semiconductor substrate;

a trench having substantially upright vertical sidewalls and a bottom surface formed in the semiconductor substrate intermediate the source and drain regions;

a channel region formed in the semiconductor substrate beneath the bottom surface of the trench and immediately contiguous the source and drain regions;

a trench-to-gate insulating layer formed on the sidewalls and bottom of the trench;

a trenched floating gate electrode having a top surface and formed inside the trench on the trench-to-gate insulating layer;

an inter-gate dielectric layer formed on the top surface of the trenched floating gate electrode; and

a control gate electrode formed on the inter-gate dielectric layer;

wherein the source region and drain region are each disposed contiguous portions of the sidewalls and of the bottom of the trench.

9. The semiconductor transistor of claim 8 further comprising:

sidewall dopings of the first conductivity type disposed immediately contiguous the substantially upright vertical sidewalls of the trench and laterally spacing each of the source and drain regions from the trench.

10. The semiconductor transistor of claim 8 wherein the top surface of the trenched gate electrode is substantially planar to the top surface of the semiconductor substrate.

11. A semiconductor substrate comprising an array of multiple device structures, each device structure spaced from other device structures and comprising:

a source diffusion region of one conductivity type formed in the semiconductor substrate;

a drain diffusion region of the one conductivity type formed in the semiconductor substrate spaced from the source diffusion region;

a trench region formed in the semiconductor substrate intermediate the source and drain diffusion regions;

a first layer of insulating material formed in said trench region;

a first gate electrode disposed in the trench region and formed on the first layer of insulating material and having a top surface;

a second layer of insulating material formed on the semiconductor substrate and disposed on the top surface of the first gate electrode for electrically isolating the first gate electrode; and

a second gate electrode formed on the second layer of insulating material.

12. The semiconductor device of claim 11 wherein the one conductivity type is n-type.

13. The semiconductor device of claim 11 wherein the one conductivity type is p-type.

14. The semiconductor device of claim 11 further comprising sidewall dopings of a second conductivity type opposite the one conductivity type, formed in the semiconductor substrate immediately contiguous the substantially vertical sides of the trench and laterally spacing each of the source and drain regions from the trench.

15. The semiconductor device of claim 11 further comprising a first sidewall doping region and a second sidewall doping region, each of a second conductivity type opposite

the one conductivity type, formed in the semiconductor substrate, with first sidewall doping region disposed between the trench region and the source region, and with said second sidewall doping region disposed between the trench region and the drain region.

16. A method for fabricating a semiconductor device with a trenched gate comprising:

etching a trench having substantially upright vertical sidewalls and a bottom surface in a semiconductor substrate;

forming a trench-to-gate insulating layer inside the trench;

forming a trenched gate electrode on the trench-to-gate insulating layer inside the trench;

forming a source region and a drain region in the semiconductor substrate;

forming an inter-gate dielectric layer on a top surface of the trenched gate electrode; and

forming a control gate electrode on a top surface of the inter-gate dielectric layer.

17. The method of claim 16 wherein the step of forming a trenched gate electrode further comprises the steps of:

depositing a layer of polysilicon on the trench-to-gate insulating layer inside the trench: and

planarizing the layer of polysilicon to substantially planar orientation with a top surface of the semiconductor substrate.

18. The method of claim 16 further comprising the step of implanting the semiconductor substrate to form sidewall dopings in the substrate laterally spacing each of the source and drain regions from the trench.

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19. The method of claim 16 wherein the step of forming a source region and a drain region comprises a self-limiting diffusion process.

20 The method of claim 16 further comprising, after etching the trench in the semiconductor substrate, forming sidewall dopings in the semiconductor substrate by implanting the semiconductor substrate with dopant impurities at an angle which is approximately between 15 and 75 degrees.

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